REMARKS

Claims 2-6 and 24-34 are pending in the present application. Replacement claims 2, 3, 24 and 30 have been presented herewith. Also, claims 31-34 have been presented herewith.

Information Disclosure Statement

Applicant respectfully acknowledges the Examiner's courtesy in requesting an in-house U.S. Patent Office translation of the "Semiconductor World" publication, and that the translation will be considered, made of record in the present application and a copy thereof provided to Applicant.

Claim Rejections-35 U.S.C. 103

Claims 2-6 and 24-30 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of the Doan et al. reference (U.S. Patent No. 5,946,595), the Besser et al. reference (U.S. Patent No. 6,165,903) and the Xiang et al. reference (U.S. Patent No. 6,015,752). This rejection, insorfar as it may pertain to the presently pending claims, is traversed for the following reasons.

Although Applicant does not necessarily concede that the above noted rejection is proper, claim 24 has been amended in order to expedite prosecution of this application. The method for fabricating a semiconductor device of claim 24 includes in combination doping an impurity into the supplemental silicon layer, "said doping

comprising doping the impurity into the supplemental silicon layer so that only the supplemental silicon layer formed over the p-channel MOS transistor is doped, or so that only the supplemental silicon layer formed over the n-channel MOS transistor is doped". Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose or make obvious these features.

As described on page 22 of the present application with respect to Figs. 6A-6C, the impurity is doped into supplemental silicon layer 536 in one of the n- and p-channel regions, so that the silicide reaction between the n-channel region and the p-channel region can be well controlled. The prior art as relied upon by the Examiner does not suggest these features and advantages.

On page 7 of the current Final Office Action dated August 12, 2002, the Examiner has alleged that a p-type source/drain with a thin polysilicon strap as shown in the Doan et al. reference would obviously have to be doped p-type to form an excellent ohmic contact and to avoid p-n diode formation, and that such reasoning would similarly hold for an n-type source/drain region connecting strap. However, this reasoning would not provide the necessary motivation for doping an impurity into a supplemental silicon layer so that only the supplemental silicon layer formed over a p-channel MOS transistor is doped, or so that only the supplemental silicon layer formed over an n-channel MOS transistor is doped. This reasoning would not provide the necessary motivation to modify the prior art as relied upon by the Examiner, so that the silicide reaction between the n-channel region and the p-channel region can be well

controlled. Although the prior art as relied upon by the Examiner may very generally suggest CMOS technology, specific description or motivation has not been established to selectively dope the supplemental silicon layer over only an n-channel MOS transistor, or to selectively dope the supplemental silicon layer over only a p-channel MOS transistor. In other words, motivation has not been established to only dope the supplemental silicon layer over one MOS transistor of a CMOS transistor pair, instead of doping the supplemental silicon layer over both transistors of a CMOS transistor pair.

Accordingly, Applicant respectfully submits that the method for fabricating a semiconductor device of claim 24 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 24-29, is improper for at least these reasons. Applicant also respectfully submits that this rejection, insofar as it may pertain to claims 2-6 and 30, is improper for at least somewhat similar reasons.

Claims 31-34

Applicant respectfully submits that claims 31-34, as respectively dependent upon claims 24 and 30, distinguish over and would not have been obvious over the prior art relied on by the Examiner for at least the same reasons as set forth above, and by further reason of the features therein.

Conclusion

The Examiner is respectfully requested to enter the above noted amendments, which should place the application in condition for allowance. The Examiner is further respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

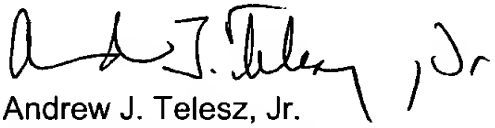
In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to December 12, 2002 for the period in which to file a response to the outstanding Office Action. The required fee of $110.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



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Enclosures: Version with Marked-Up Changes

VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Claims:

2. (Four Times Amended) The method according to claim 30, wherein the material to be silicided [metal layer] comprises cobalt.

3. (Four Times Amended) The method according to claim 30, wherein the material to be silicided [metal layer] comprises titanium.

24. (Three Times Amended) A method for fabricating a semiconductor device, comprising:

providing a semiconductor substrate which has a silicon region located on an insulating layer formed in the semiconductor substrate;

forming a metal layer on the silicon region of the semiconductor substrate;

performing a first rapid thermal annealing on the semiconductor substrate to form first-reacted silicide regions;

forming a supplemental silicon layer on the first-reacted silicide regions;

doping an impurity into the supplemental silicon layer; and

performing a second rapid thermal annealing to convert the first-reacted silicide regions into second-reacted silicide regions, by reaction of the supplemental silicon layer with the first-reacted silicide regions,

the semiconductor device including a p-channel MOS transistor having p-type

source and drain diffusion layers, and including an n-channel MOS transistor having n-type source and drain diffusion layers,

said doping comprising doping [a p-type] the impurity into the supplemental silicon layer so that only the supplemental silicon layer [is] formed over the p-channel MOS transistor is doped, or so that only [and doping an n-type impurity into] the supplemental silicon layer [that is] formed over the n-channel MOS transistor is doped.

30. (Amended) A method for fabricating a semiconductor device comprising:

providing a silicon substrate;

providing a buried oxide layer on the silicon substrate;

providing a field oxide layer and a silicon on insulator layer on the buried oxide layer;

providing a gate oxide layer on the silicon on insulator layer;

providing a poly-silicon gate layer on the gate oxide layer;

providing a gate side wall layer on the silicon on insulator layer to surround the poly-silicon gate layer and the gate oxide layer;

providing a material to be silicided on a surface of the semiconductor device including the poly-silicon gate layer, the gate side wall layer, the silicon on insulator layer and the field oxide layer;

performing a first rapid thermal annealing process to form first-reacted silicide regions in the poly-silicon gate layer and in source/drain active areas of the silicon on insulator layer;

removing non-reacted material from the first-reacted silicide regions;

providing a supplemental silicon layer over the surface of the semiconductor device after the non-reacted material is removed;

doping the supplemental silicon layer; and

performing a second rapid thermal annealing process to convert the first-reacted silicide regions into second-reacted silicide regions, by reaction of the supplemental silicon layer with the first-reacted silicide regions,

the supplemental silicon layer preventing the poly-silicon gate layer and the silicon on insulator layer from being completely silicided,

the semiconductor device including a p-channel MOS transistor having p-type source and drain regions, and including an n-channel MOS transistor having n-type source and drain regions,

said doping comprising doping an [a p-type] impurity into the supplemental silicon layer so that [is] only the supplemental silicon layer provided over the p-channel MOS transistor is doped, or so that only [and doping an n-type impurity into] the supplemental silicon layer [that is] provided over the n-channel MOS transistor is doped.